Design Techniques Enhance Isolaiton In Switch Assemblies

By paying attention to PCB layout concerns, high isolation is achieved with low-cost, of-the-shelf MMIC components.

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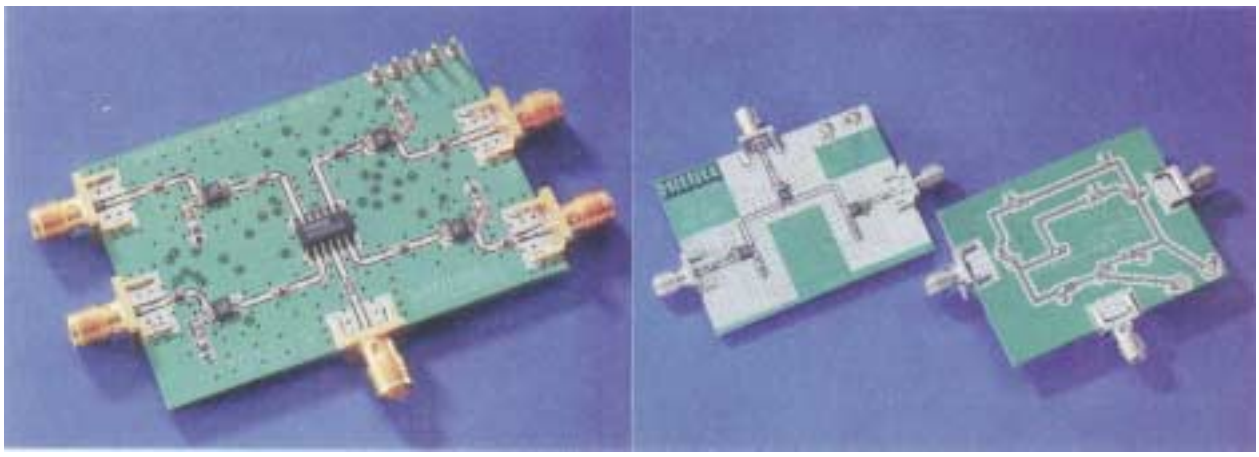
Channel switching represents a key function in cellular and parsonal-communications-services (PCS) base-station applications. This switching may be implemented in various sections of a system - for instance, between the trasnmit and receive paths, betwen multiple local-oscillator (LO) sources, or between antennas. A certain amount of isolation is required between paths, with this isolation requirement often being up to 60 dB (in some cases, more than 100 dB). In addtion, commercial applications require small, low-cost solutions. Consequently, it is desirable to implement switching matrices using standard, off-the-shelf monolithic-microwave0intergrated-circuit (MMIC) components in plastic packages. Guidelines for designing high-isolation RF switching matrices with standard components - including printed-circuit-board (PCB) layout techniques for minimizing secondary effects such as coupling, radiation, and leakage - are examined using two switch assemblies developed by Htiite Microwave Corp. (Chelmsford, MA).

Both designs (Fig. 1) use low-cost multilayer FR4 substrates. The first is a four-channel antenna selection matrix which provides 65-dB channel rejection across an operaing frequency range of 100 MHz to 2 GHz. This circuit (Fig. 2) employs four positive-control HMC190MS8 single-pole, double-throw (SPDT) switches and a single negative-control HMC182S14 single-pole, four-throw (SP4T) switch with an on-chip 2:4 decoder. A 2-b complementary-metal-oxide-semiconductor (CMOS)-compatible level-



1. This four-channel antenna selection matrix (left) and two-channel LO selection circuit (right) operate across a frequency range of 100 MHz to 2 GHz.

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Table 1: Isolation versus switch spacing

Layout	Short	Medium	Long
Transmission-line length between switches	0.7 in.	0.8 in.	0.9 in.
Mean isolation (no shielding; 1 to 2 GHz)	75.6 dB	77.6 dB	79.7 dB
Change in isolation with increasing line length	0.0 dB	+2.0 dB	+4.1 dB

shifter/decoder circuit (using Zener diodes) is also incorporated, with CMOS logic gates to drive the five MMIC switches. Positive and negative supply voltages (±5 VDC) are required.

The second design is a high-isolation (>90 dB) two-channel LO selection circuit which also operates from 100 MHz to 2 GHz. This circuit uses three positive-control HMC194MS8 SPDT switches and requires only two control lines (Fig. 3). Each of the HMC194MS8 switches is capable of delivering 40-to-50-dB isolation up to 2 GHz. By using proper layout techniques, isolation levels from 90 to more than 100 dB are achieved in a SPDT assembly formed with only three swithces.

LRM CALIBRATION

In order to design an Rf system using multiple package MMIC com- ponents, accurate S-parameter data must be obtained for the individual components. This is best accomplished by designing a custom evaluation printed-circuit board (PCB) and a set of LRM (line, reflect, match) calibration standards for each of the components. These standards typically consist of a zero-length through, an open or short, and a 50-Ohm load on the same layout as the evaluation PCB traces.

LRM calibration standards have been developed for several products at Hittite Microwave, including the HMC182S14, HMC190MS8, and HMC194MS8 switches. These standards support de-embedding directly to the leads of the plastic MMIC packages. This approach is considerably more accurate than other common de-embedding methods since it accounts for actual PCB mismatches, line losses, and blocking-capacitor losses. However, there may be small errors associated with slight differences between the calibration and evaluation PCBs due to processing tolerances.

Using LRM calibration, two-port S-parameter data was obtained for each operating state of every product. For instance, an SPDT switch such as the HMC194MS8 possesses four two-port data sets corresponding to the “ON” and “OFF” states along both switch paths.

RF CIRCUIT MODEL

A simple model for the desired system or subsystem can be constructed with the Libra simulation package fromt he Hewlett-Packard HP-EEs of Division (Westlake Village, CA) by using the two-port de-embedded S-Parameters for the packaged MMICs. This model takes into account only the direct RF paths - neglecting the radiation, coupling, and leakage which may

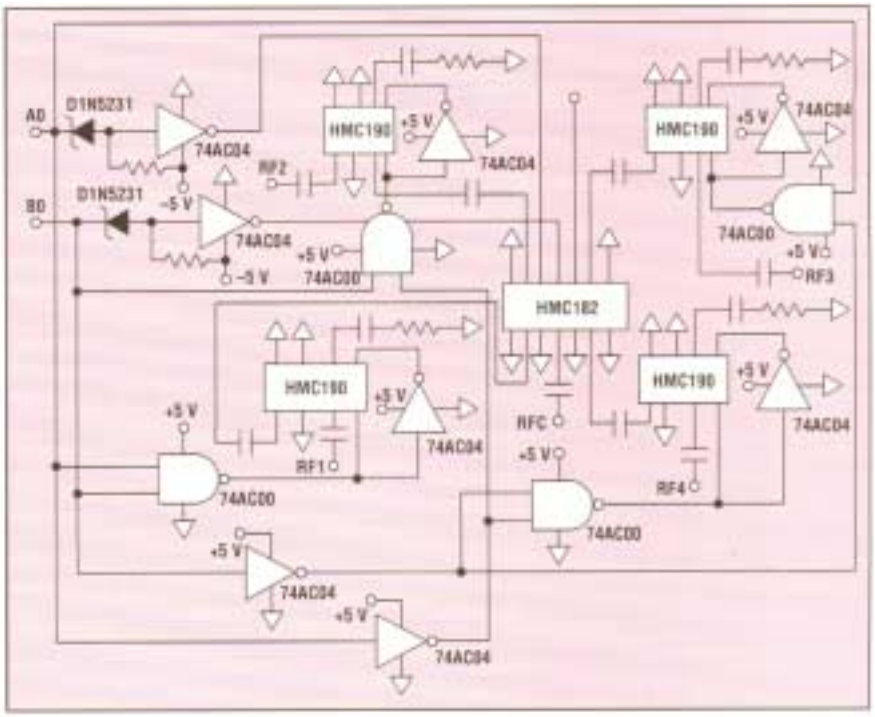

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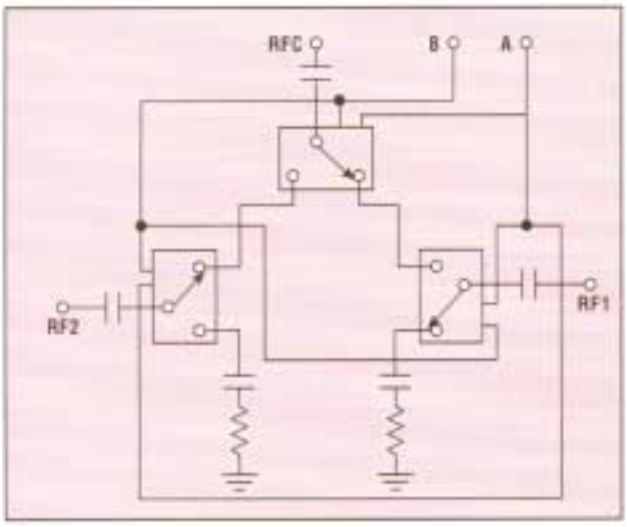
Table 2: Four-channel antenna switching matrix performance		
	900 to 1000 MHz	1800 to 2000 MHz
Return loss	18 dB	14 dB
Isolation	65 dB	65 dB
Insertion loss	1.4 dB	1.8 dB



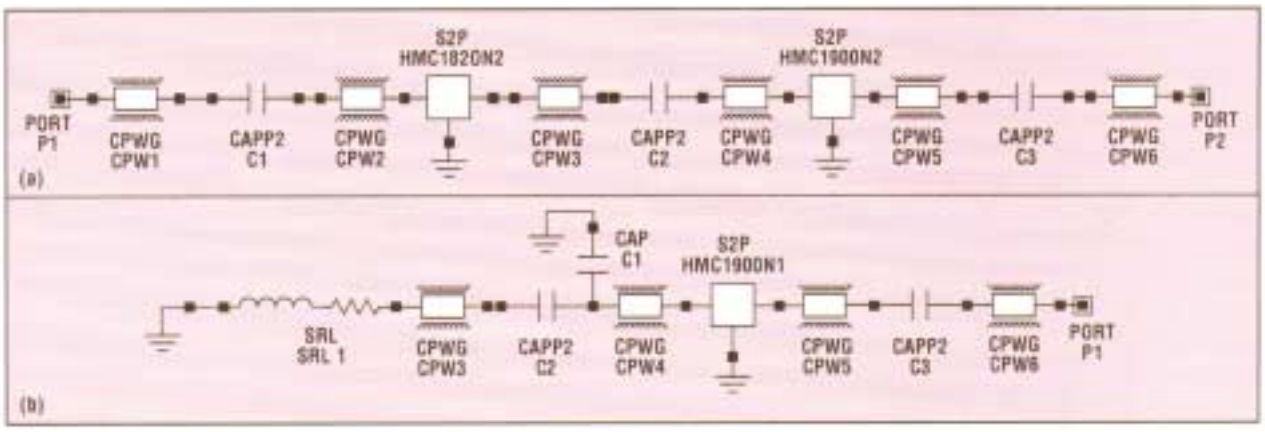
3.This two-channel Lo selection circuit provides better than 90-dB isolation while requiring only two control lines.

occur (these secondary effects will be addressed later). The model may be as simple as a few 50-Ohm lines attached to the input and output of a single two-port data block or as extensive as the cascading of multiple two-port data blocks for different packaged MMICs as well as transmission lines, blocking capacitors, and other RF components. For a switching matrix, there will be Libra models for the ON (through) and OFF (isolated) states along each path of the matrix. For single-pole, N-throw (SPNT) switch matrices, there will be multiple OFF state models corresponding to the isolation between two channels when each of the other channels is selected. Designers may wish to use only the data for the worst-case path, as this greatly reduces the amount of required data.

For these switch-matrix designs, the Libra simulation incorporated grounded coplanar-waveguide transmission-line models (denoted as CPWG in Libra) in order to achieve the best possible isolation for the final physical layout. The following parameters were assumed (modeling low-cost FR4 material):

- Reative dielectric constant (∈r) = 4.6
- Groun-place spacing (H) = 0.030 in. (0.762mm)
- 50-Ohm line width (W) = 0.038 in. (0.965mm)
- Coplanar gap (G) = 0.013 in. (0.330mm)
- Loss tangent (tan ∆) = 0.023 (0.584mm)
- DC-blocking capacitance = 330 pF

Figure 4 shows the Libra schematics for the four-channel antenna selection matrix. Figure 4a models the RF-common (RFC)-to-RF2 ON state. Note that the HMC190MS8 and HMC182S14 switches are replaced by the two-port S-parameter data blocks corresponding to the appropriate states for each swithc. This model is valid for all four S-parameters of the ON state. However, when constructing models for the isolation paths, the S-parameters of the over-all circuit cannot



4. These Libra models were obtained for the four-channel antenna matrix for the RFC-to-RF2 ON (a) and OFF states (b)

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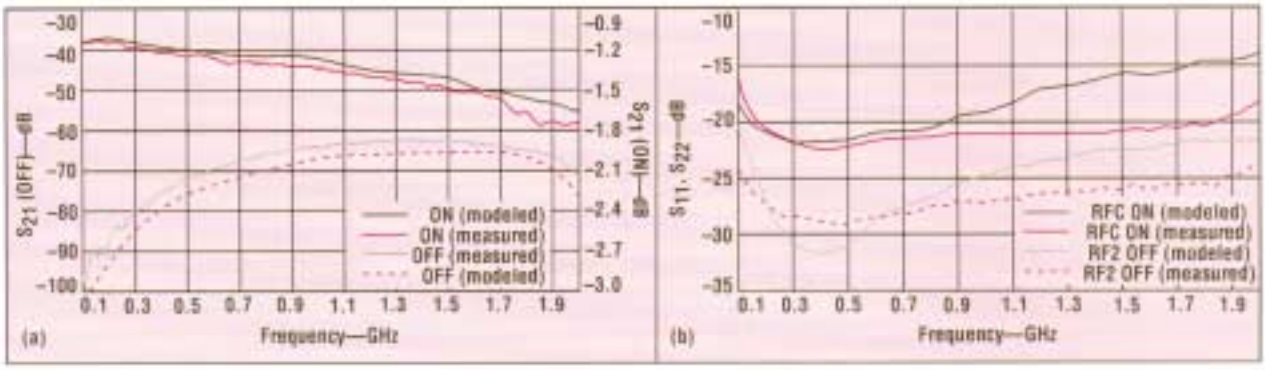


5. Simulated and measured transmission (a) and matching performance (b) are shown for the four-channel antenna selection matrix.

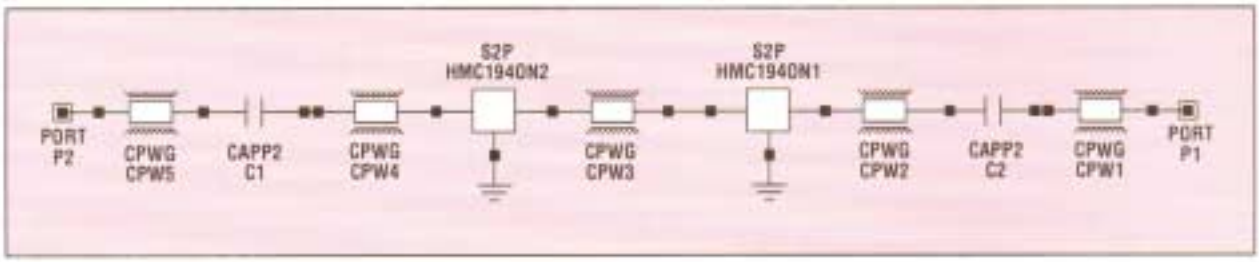
be obtained from a single schematic model. For example, referring to Fig. 2, the match at antenna 2 when it is OFF (isolated) is found by modeling a single HMC190MS8 switch whose RF1 path is selected and terminated by a 50-Ohm chip resistor. Figure 4b shows the schematic for this state.

Figure 5 presents the S-parameter response for the four-channel antenna matrix as modeled in Libra, with measured data included for comparison. The worst-case isolation is shown (corresponding to adjacent ports 2 and 3). Ths isolation between diagonal ports 2 and 4 is approximately 5 dB better, with the difference being associated with the packaging pin-out of the HMC182S14 device.

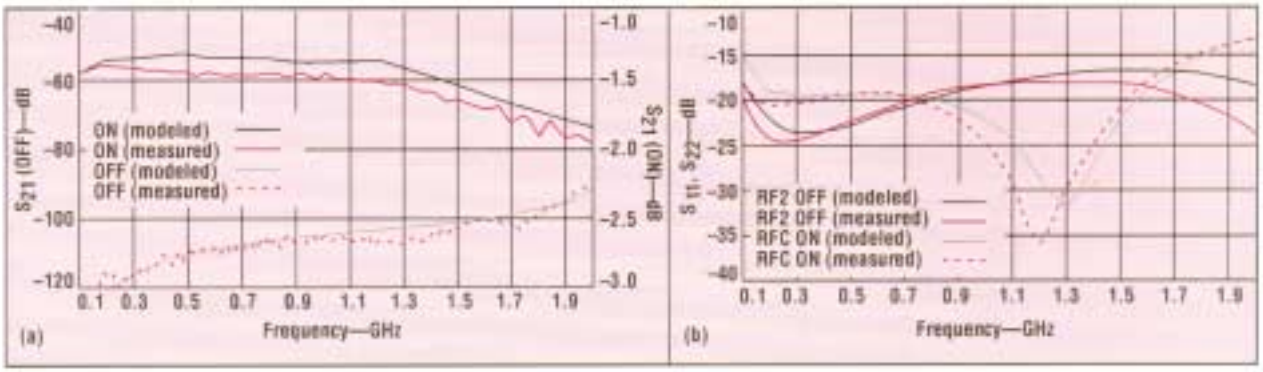
Figure 6 show the Libra schematic for the two-channel LO selector design. This schematic corresponds to the RFC-to-RF1 ON state. The model uses quarter-wavelength spacing at 2 GHz (≈ 0.7 in.) between switches to enhance isolation. Figure 7 presents the measured and modeled S-parameters.

LAYOUT GUIDELINES

There are a number of factors that are not taken into account in the simple model. These factors include radiative coupling,



6. This Libra model wa sobtained for the two-channel LO selection matrix in the RFC-to-RF1 ON state.



7. Measured as well as simulated transmission (a) and matching parameters (b) were obtained for the two-channel LO selection matrix.

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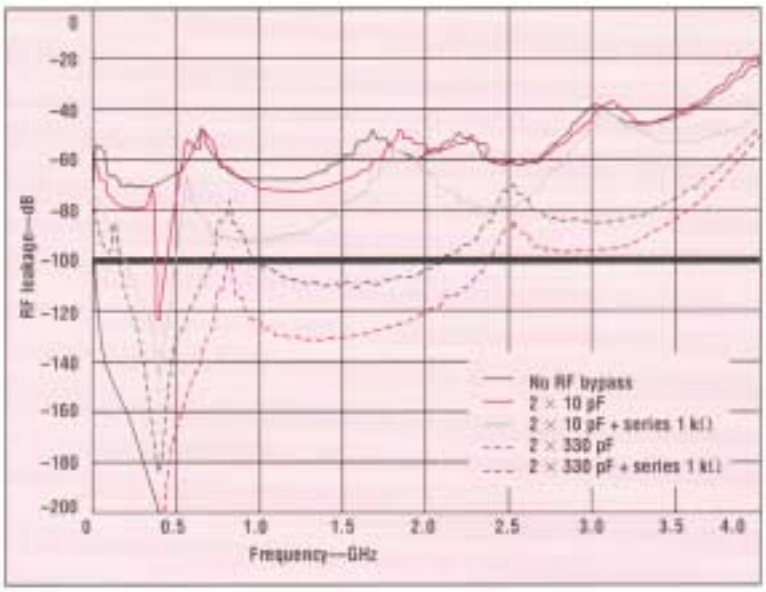
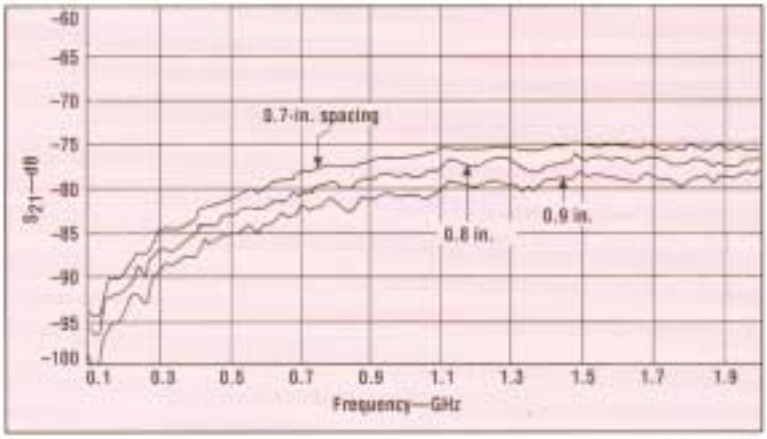


8. The effects of different RF-bypassing schemes are examined using the measured Rf leakage present at the isolated switch output.

transmission-line coupling, and Rf-to-control line leakage. In some cases, neglecting these effects may only cost a few tenths of a decibel. In other cases, the results may be devastating – on the order of 30 dB or more in terms of performance degradation. In a design where low isolation is expected (40 dB or lower), effects such as radiation and RF leakage may be masked by the inherent isolation limitation of the selected devices. However, in cases where the MMIC isolation "noise floor" is lower than 50 or 60 dB, layout-related issues become significant. Following appropriate Rf-layout guidelines can minimize or eliminate these secondary effects.

Traditional RF-layout guidelines include the use of mitered bends, adequate spacing between Rf trasmission lines, tapered transitions, maintaining proper 50-Ohm line widths, as well as proper grounding of components and connectors. However, high-isolation switching matrices require tighter layout constraints in order to achieve the performance shown in models.



9. Measurements performed on the two-channel LO selection circuit demonstrate a relationship between swithc spacing and isolation.

Both of the curcuit designs presented here use grounded-coplanar-wave-guide (CPW) transmission lines, as opposed to microstrip. There are several reasons why CPW is a desireable layout choice:

• CPW transmission lines with tight gaps support narrower lines, thereby easing layout constraints.

• CPW should reduce radiation and coupling since fringing fields above the PCB will have a top-layer ground on which to terminate.

• CPW provides a ground under all board components. By using a higher density of plated-through ground vias under components, isolation can be improved.

• CPW lines are convenient for Rf bypassing of DC and low-frequency lines since the ground plane is in close proximity to all lines – supporting placement of shunt chip capacitors.

• CPW transmission lines require far less tooling time for prototyping on circuit milling machines. This is due to most of the ground plane being left intact.

When using CPW, it is necessary to include the top and bottom ground planes. These holes must be spaced closely (λ/20 or less) relative to the wavelenght at the maximum operating frequenc. The effect of plated through holes is to channelize the signals and prevent "hot spots" on the coplanar ground.

Another recommended layout technique is the use of a multilayer PCB. All of the designs persented here use a four-layer PCBs fabricated at Circuit Board Express (Haverhill, MA). There are two key reasons why this is desirable:

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Table 3: Two-channel LO selection circuit performance		
	800 to 1000 MHz	1800 to 2000 MHz
Return loss	17 dB	14 dB
Isolation	105 dB	92 dB
Insertion loss	1.5 dB	2.0 dB

• Two-layer boards may result in DC and low-frequency lines dividing the RF ground plane, so that various components will not share a common ground. If multiple layers are used, the metal layer directly below the RF traces may be kept intact to achieve a continuous RF ground plane.

• A standard total PCB thickness of 0.062 in. (1.57mm) guarantees a mechanically sturdy design and provides compatibility with standard PCB edge-mount connectors. However, using an RF-ground-plane spacing of 0.062 in. is not desirable because of the wide line widths required. A multilayer PCB enables the RF ground-plane spacing to be kept small, whille the overall layer stack-up still remains mechanically favorable.

USING A MULTILAYER BOARD PROVIDES SEVERAL ADVANTAGES, INCLUDING THE ABILITY TO MAINTAIN A CONTINUOUS RF GROUND PLANE AND SMALL GROUND-PLANE SPACING.

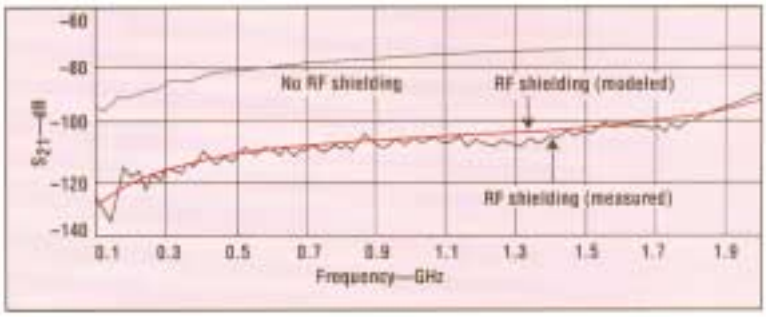
The benefit of using a multilayer topology is demonstrated by the four-channel antenna selection matrix from Fig. 2. In that design, all of the RF components were placed on metal layer 1 while all of the control-logic components were placed on metal layer 4. The control-logic traces are on metal layers 3 and 4, while metal layer 2 is left intact as an RF ground plane.

MINIMIZING LEAKAGE

In addition to the RF input and output pins, packaged MMIC switches often contain a number of DC or low-frequency control and supply pins. Due to pin-to-pin coupling, bond-wire coupling, and RF leakage within the MMIC components, a small RF level will be present at these non-RF pins. In the PCB layout, it is possible to minimize the effects of this leakage by placing RF-bypass capacitors on all DC and low-frequency lines. Thses bypass capacitors should be as close to the RF leakage source as the layout will allow – ideally directly at each MMIC control or supply pin. If the RF–bypass capacitors are too far from the leakage sources, the RF leakage may radiate or couple to other structures in the circuit.

Leakage between parts may be further reduced by placing series resistors on the control lines and by adding bypass capacitors on long traces between switches. A model was constructed in order to demonstrate the effect of this leakage n the performance of a high-isolation circuit. Using a test fixture with SMA connectors, the S-parameters between the RFC and the A and B control lines of the HMC194MS8 SPDT switch were measured. This measurement was performed by using a bias tee to inject DC onto the control line. The insertion loss due to RF leakage was approximately 25 to 30 dB at 2 GHz.

Next, the measured RF-to-control S-paremeter data was used to obtain a Libra model for a single length of control line between two switches on the two-channel LO selection circuit. Figure 8 shows the RF level present at the isolated switch output due to the leakage on this single control line for four different bypassing schemes. For high-isolation cellular or PCS applications, RF bypassing of 330 pF with a series 1-k Ohm resistor on each control line is recommended.



10. The isolation performance of the two-channel LO selection circuit is significantly improved by employing Rf shielding.

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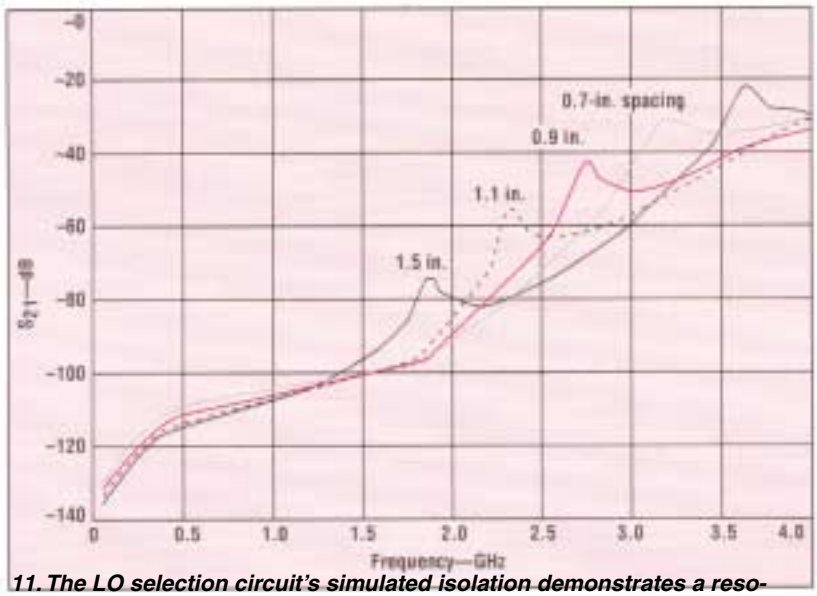

11. The LO selection circuit's simulated isolation demonstrates a resonance that moves down in frequency a sthe switch spacing increases.

There is, however, a trade-off between switching speed and isolation – governed by τ = RC (where τ is the switching time constant, R is resistance, and C is capacitance). The largest possible bypass capacitors which still meet the switching-speed requirements should be selected in order to maintain a low-impedance path to ground. This is particularly important in the lower frequency range since the impedance (Z) of a capacitor is governed by Z = 1/jωC (where ω is the radian frequency).

Radiative coupling is a critical factor in applications requiring extremely-high isolation. When a transmission line terminates at the pin of a packaged component, most of the signal is either launched into the device or reflected. However, the non-ideal nature of the transition will result in a small fraction of the power being radiated. In effect, the transition behaves like an antenna (fortunately, an extremely inefficient one). The intensity of the radiation decreases rapidly with distance. However, some of the radiation may couple into the circuit. This can occur in undesirable locations, such as the isolated path of a switch matrix.

A demonstration of the effects of radiative coupling was performed. Three versions of the two-channel LO selection circuit were built – with the transmission-line spacing between switches at 0.7, 0.8, and 0.9 in. (1.78, 2.03, and 2.29 cm), respectively. Figure 9 compares the measured isolation for each design while Table 1 presents the mean isolation in the boards.

There is a direct relationship between switch spacing and isolation. Note that in all three cases shown in Fig. 9, the isolation performance falls far short of the modeled data from Fig 7a. This discrepancy is primarily due to channel-to-channel radiative coupling. To minimize this effect, it is necessary to use RF shielding covers. By enclosing each switch in a small housing, the radiation between channels is almost totally eliminated, improving isolation performance by more than 25 dB (Fig 10). The RF shields used are standard off-the-shelf products from Fotofabrication Corp. (Chicago,IL).

The results in Table 1 suggest postioning the switches as far apart as possible in order to improve isolation. However, this is impractical due to a resonance that moves down infrequency as the spacing between switches is increased. Fig 11 shows modeled data for the isolation performance as a function of switch spacing. When the transmission-line lenght reaches 1.5 in. (3.81 cm), the resonance is in the PCS frequency band. Consequently, there is a trade-off between reducing the radiative coupling (unshielded) and avioding this resonance. A reasonable compromise is to allow a λ/4 spacing between switches at the highest frequency of interest.

Most of the design and modeling focus has been on describing the isolated states of the switching matrices. However, there are some considerations that must be taken into account in order to develop an accurate model of the transmission states. The primary requirements are:

- Accurate line-length measurements (when back-modeling existing physical designs).
- Accurate estimation of $\in$r and tan δ.
- Valid models for DC-blocking capacitors [including quality factor (Q) and resonance frequency].

The first criteria is easy to accomplish. However, it is important because an error of a few tenths of an inch in line-length estimation can result in a few

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hundred megahertz of offset for certain performance attributes, such as nulls in the return loss or isolation.

Material parameters such as $\in$r and tan δ are generally not specified precisely for low-cost materials such as FR4. However, these parameters can be determined experimentally. Note that $\in$r affects not only the transmission-line impedance, but also the electrical length. For the Fr4 material used, the measured PCB loss for 50-Ohm lines was approximately 0.1 dB/(in.-GHz) – corresponding to a tan δ of approximately 0.023.

An accurate circuit model for the capacitors should be obtained from the manufacturer. This is critical since at high frequencies (>2 GHz), typical low-cost capacitors exhibit a roll-off in their insertion-loss performance (due to thier resonance characteristics). The modeled data given here uses the Libra CAPP2 model for non-ideal capacitors.

It may be undesirable to use Dc-blocking capacitors in high-freuency designs due to the insertion-loss roll-off induced by these devices. In the two-channel LO selection circuit, it may be possible to eliminate Dc-blocking capacitors if the system in which the circuit is used is AC-coupled. However, in the four-channel antenna selection matrix, the inter-switch DC blocking is required since the four HMC190MS8 chips and the HMC182S14 switch are operated at different logic levels. An optional design involves operating theHMC190MS8 with negative logic levels, eliminating the need for the five inter-switch DC-blocking capacitors.

Tables 2 and 3 summarize the measured performance of the SP4T antenna switching matrix and the SPDT LO-selection circuit, respectively. With two design iterations, the measured performance of the devices achieved close agreement with the modeled data. ••

Note

De-embedded S-parameters for various products, including the SPDT and SP4T switches described in this article are available on the Internet at htp://www.hittite.com.

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